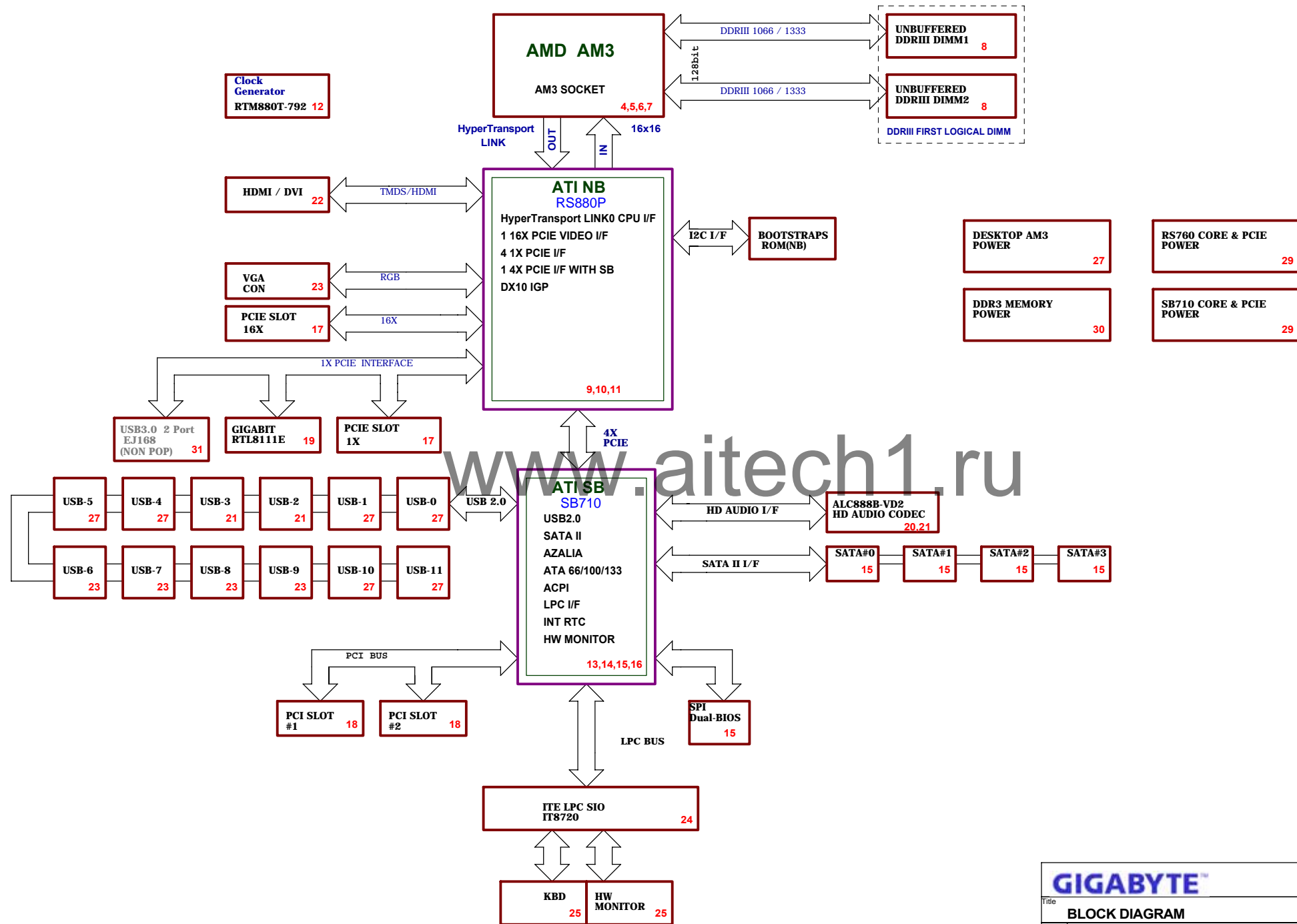


Revision : 3.11

PAGE	TITLE	9M
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU HYPER TRANSPORT	
05	CPU DDRIII MEMORY	
06	CPU CONTROL	
07	CPU POWER & GND	
08	DDRII CHANNEL A0,B0	
09	RS880 HT-LINK I/F PCIE I/F	
10	RS880 SYSTEM I/F STRAP	
11	RS880 POWER & GND	
12	RTM880-792	
13	ATI SB710 PCIE/PCI/CPU/LPC	
14	ATI SB710 ACPI/USB/GPIO/AUDIO	
15	ATI SB710 SATA/SPI/IDE/HWM	
16	ATI SB710 POWER & GND	
17	PCI EXPRESS x16 ,x1	
18	PCI SLOT 1, 2	
19	REALTK RTL8111E	
20	ALC888B	
21	AUDIO JACK	
22	IDE ,FDD ,HDMI ,DVI Connector	
23	RGB Connector COM/LPT/F_USB	
24	IT8720 LPC IO ,Dual-BIOS	
25	FAN/HWMO ,KB/USB	

[illegible]

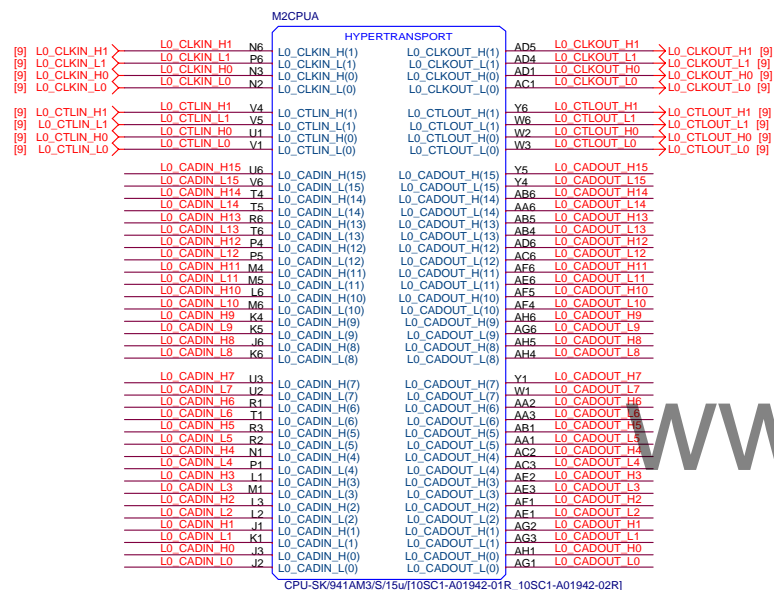
RS880 CUSTOMER DESKTOP REFERENCE DESIGN



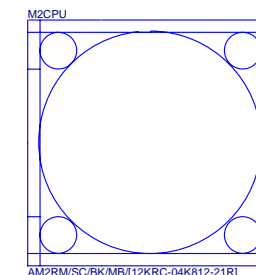
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L0_CADIN_H[0..15] < L0_CADIN_H[0..15] [9]
L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] [9]
L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] [9]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

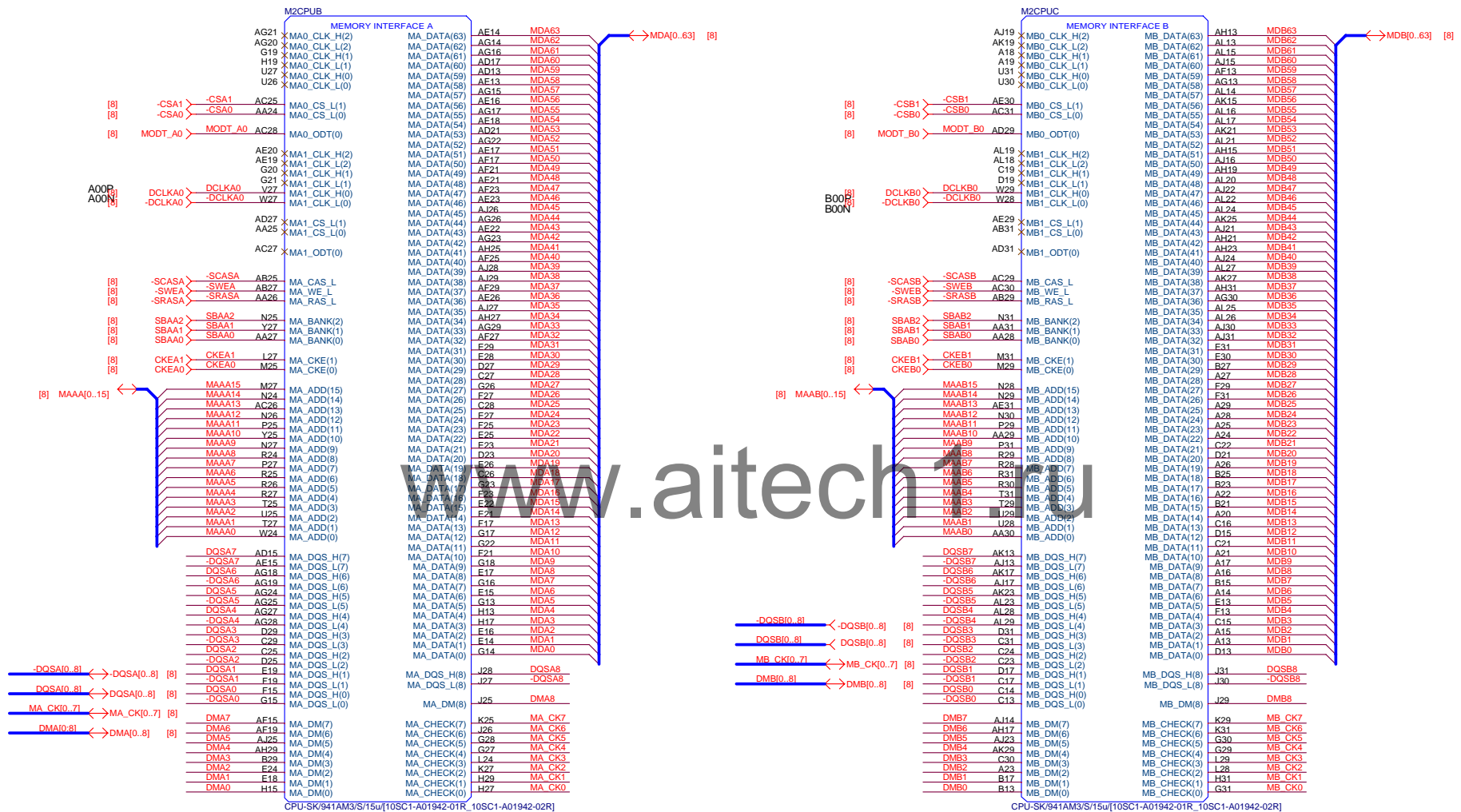


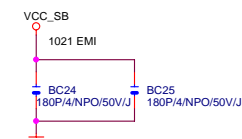
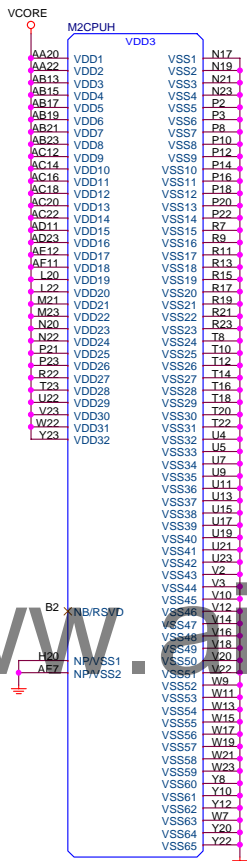
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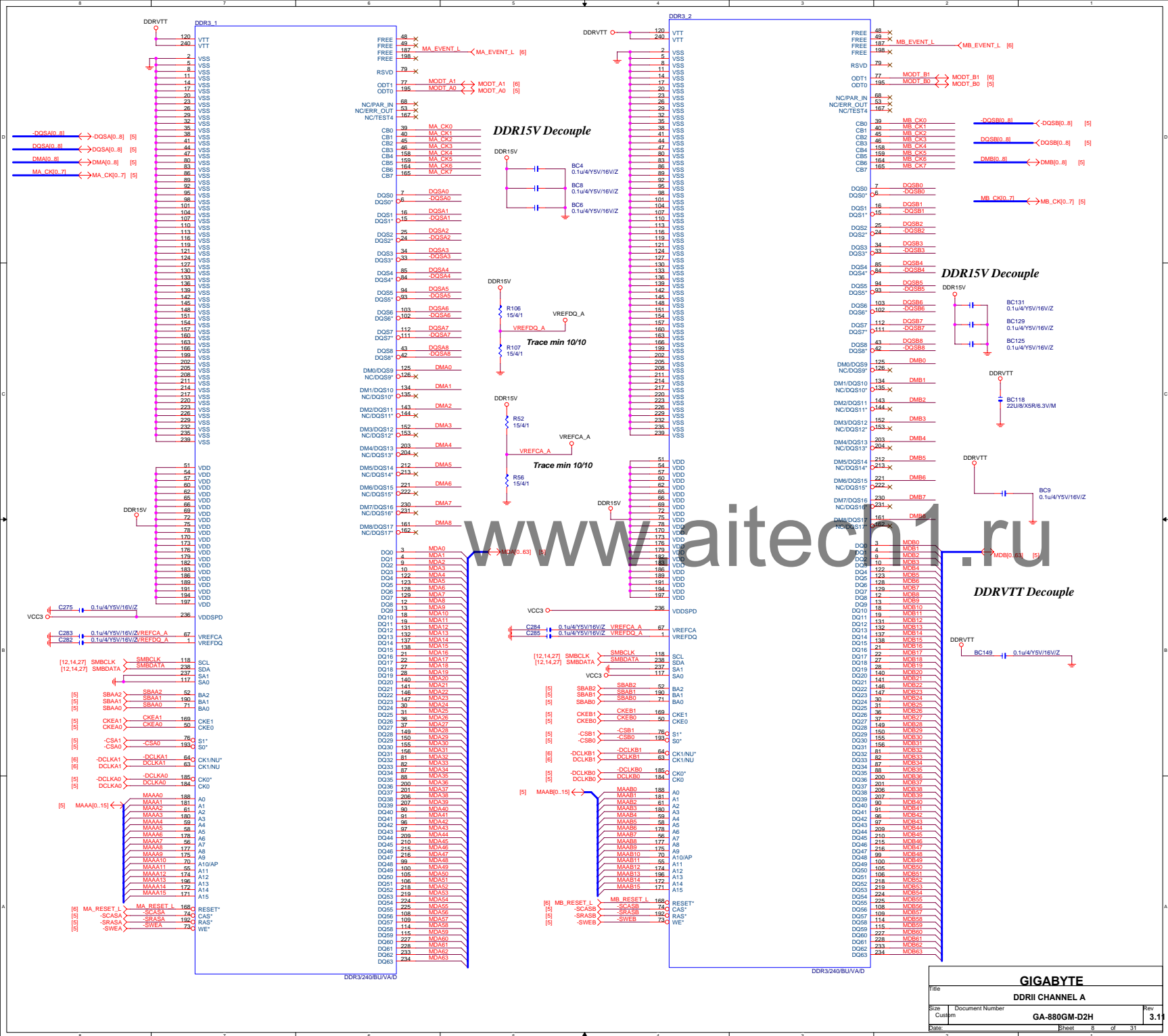


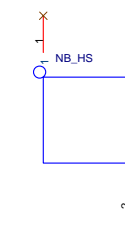
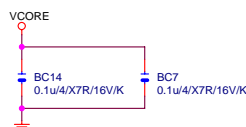
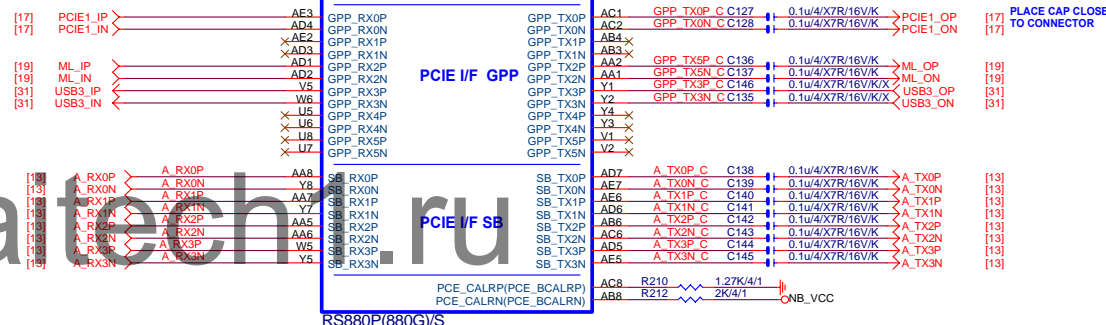
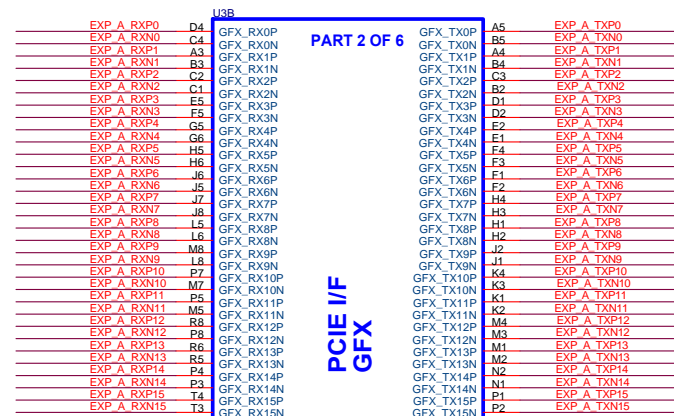
GIGABYTE

Title			
CPU HYPER TRANSPORT			
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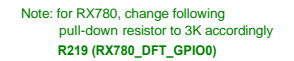


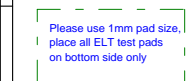




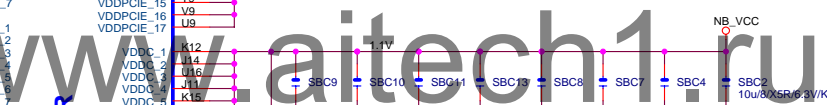


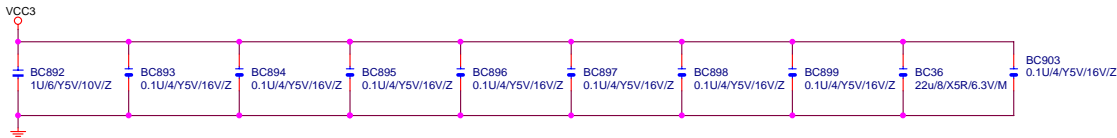
Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly





PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD03	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

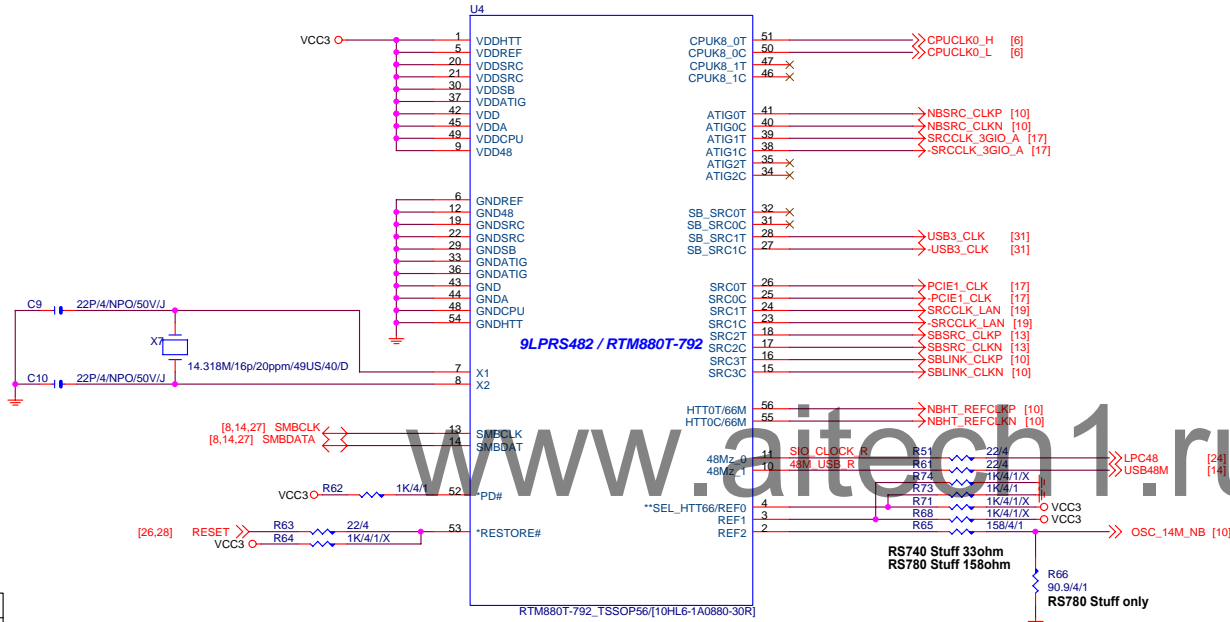
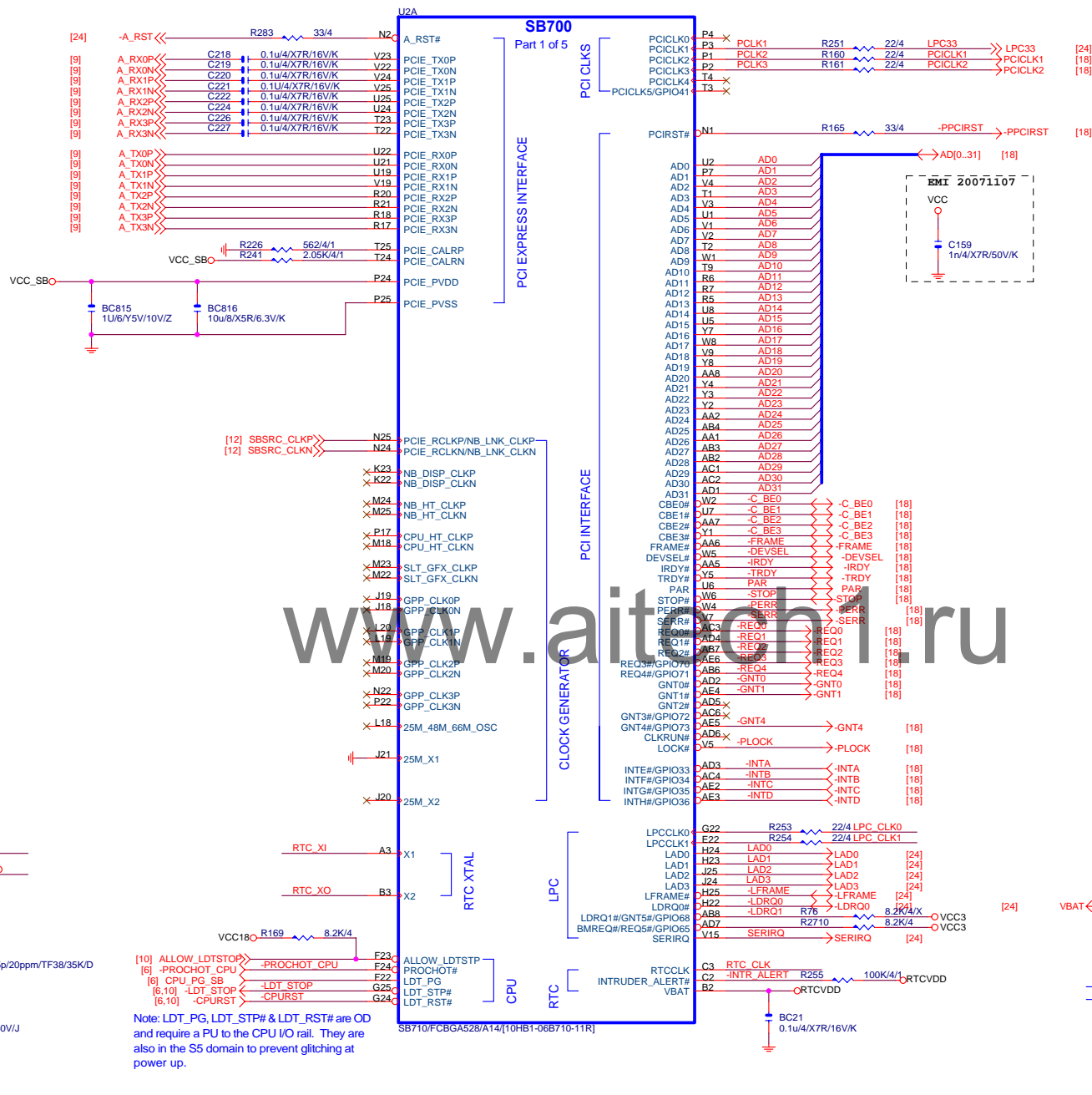


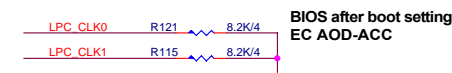


Diagram illustrating a square structure. The top-left vertex is labeled 1, and the bottom-right vertex is labeled 2. The label SB_HS is positioned near the top-left vertex.

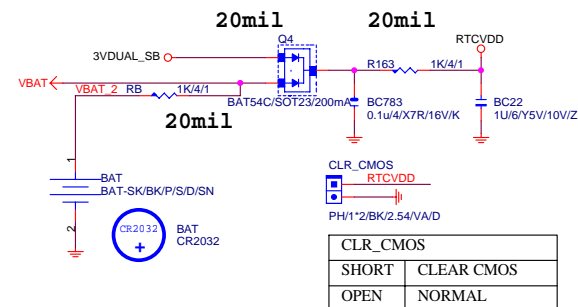
SB_HS/[12SP2-030030-51R_12SP2-030030-53R]
SB HS Modify by Eric Request



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT



	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT



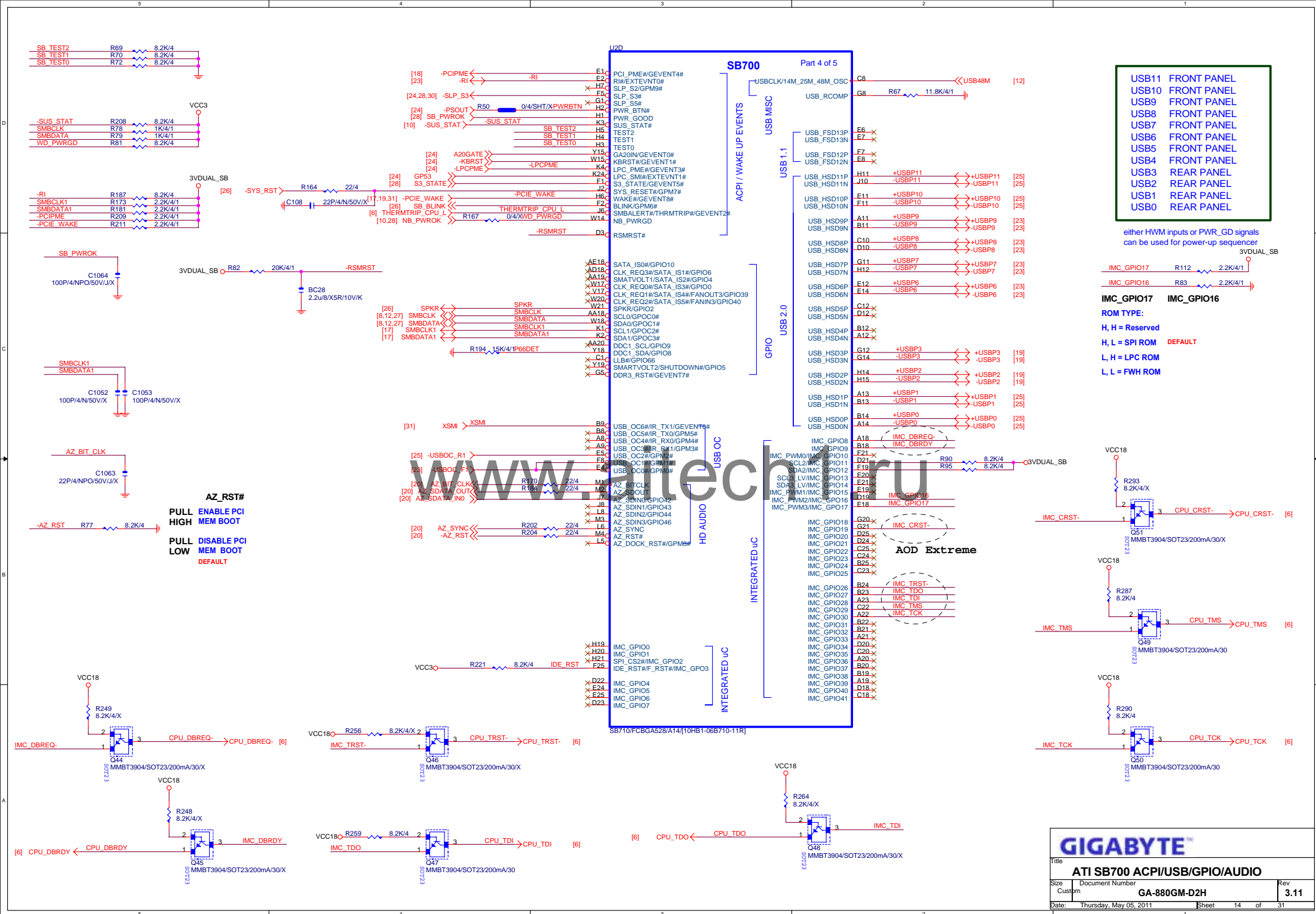
NOT ADD ICT FOR RTCVDD PIN

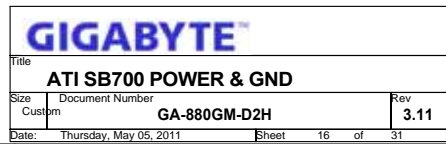
GIGABYTE™

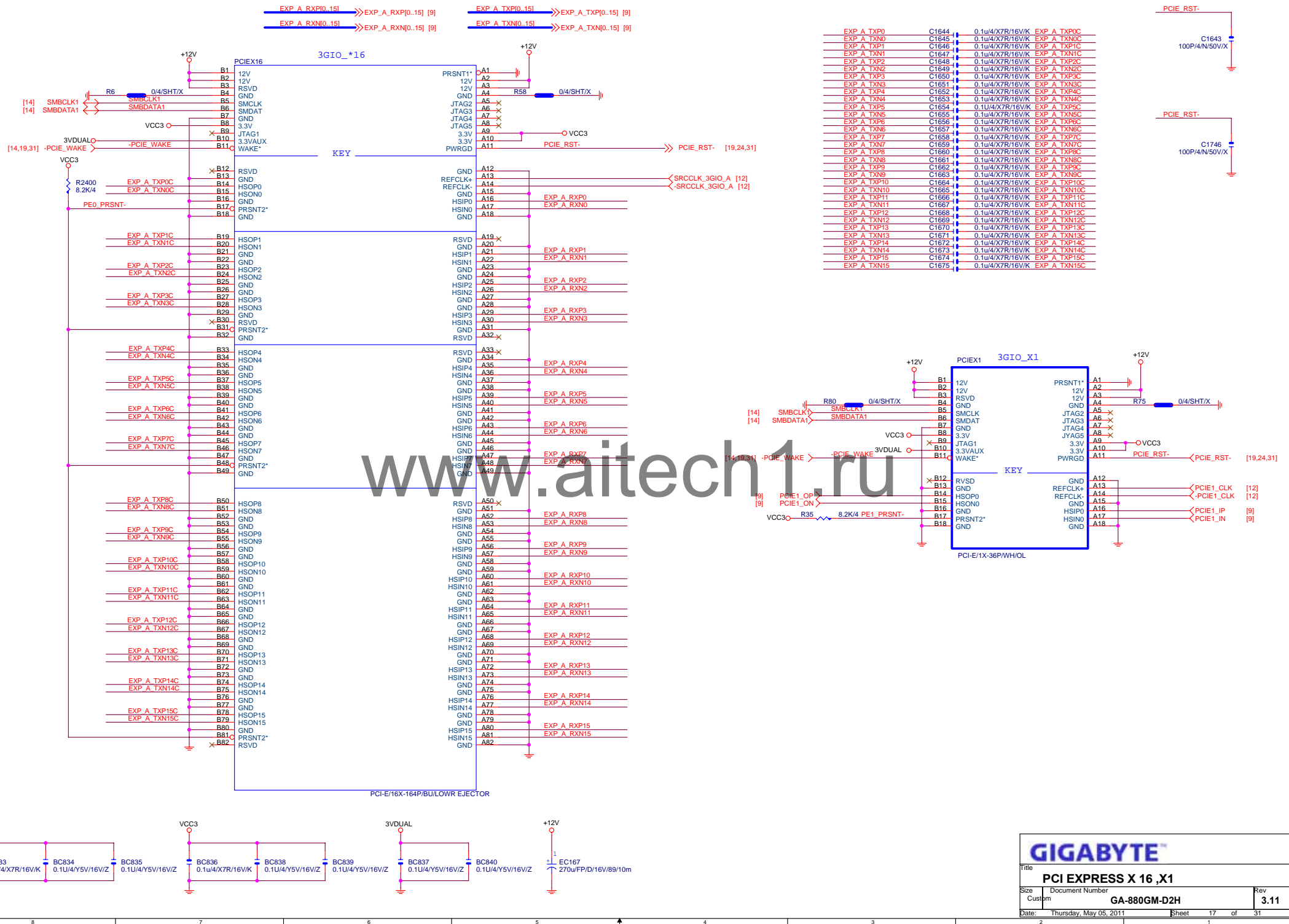
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Size	Document Number	Rev
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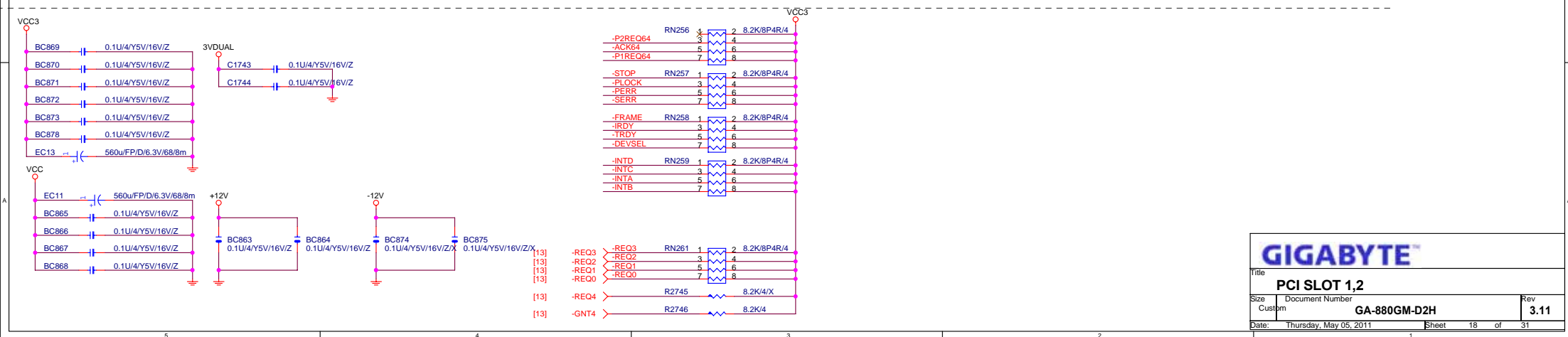
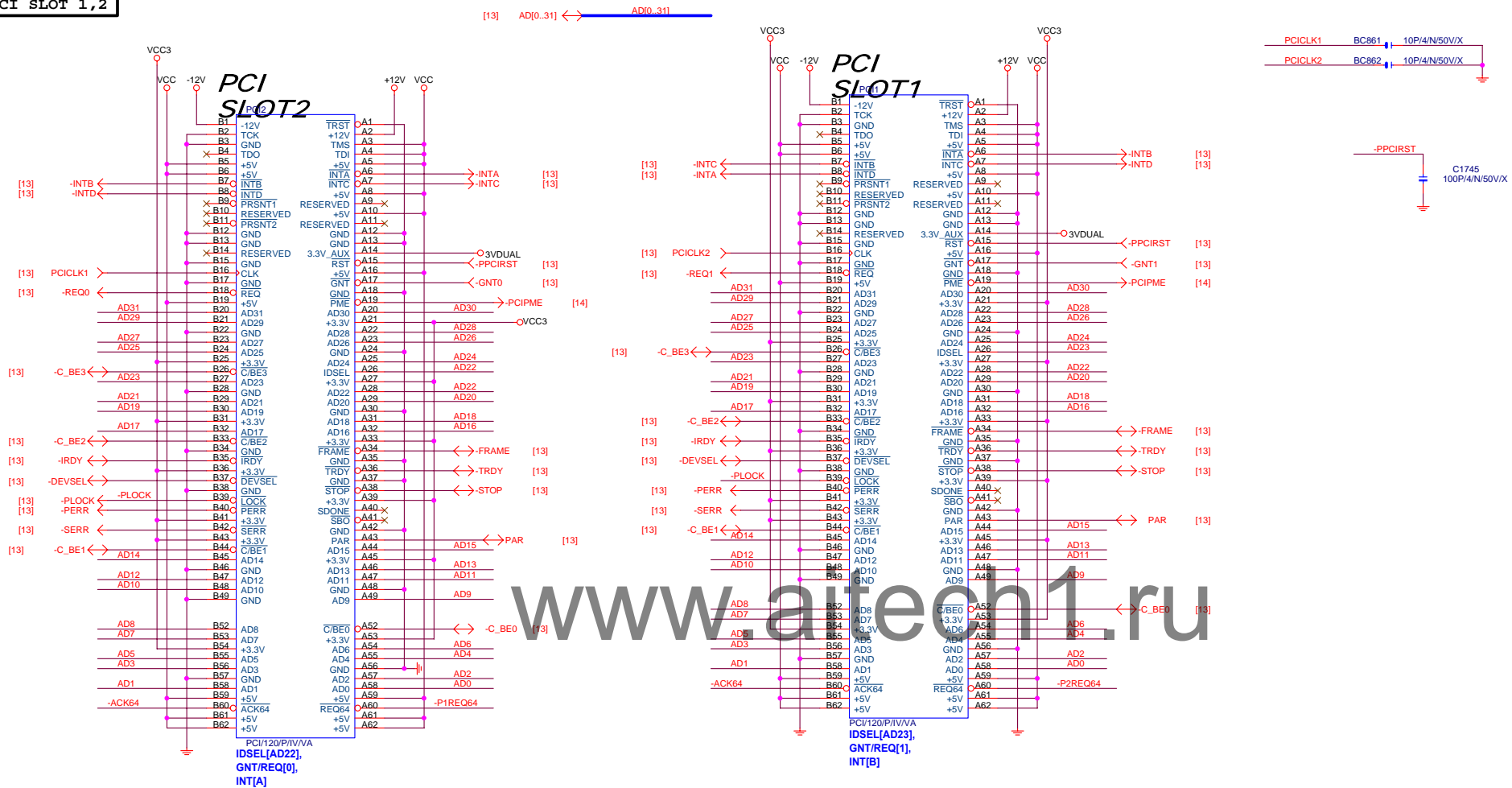
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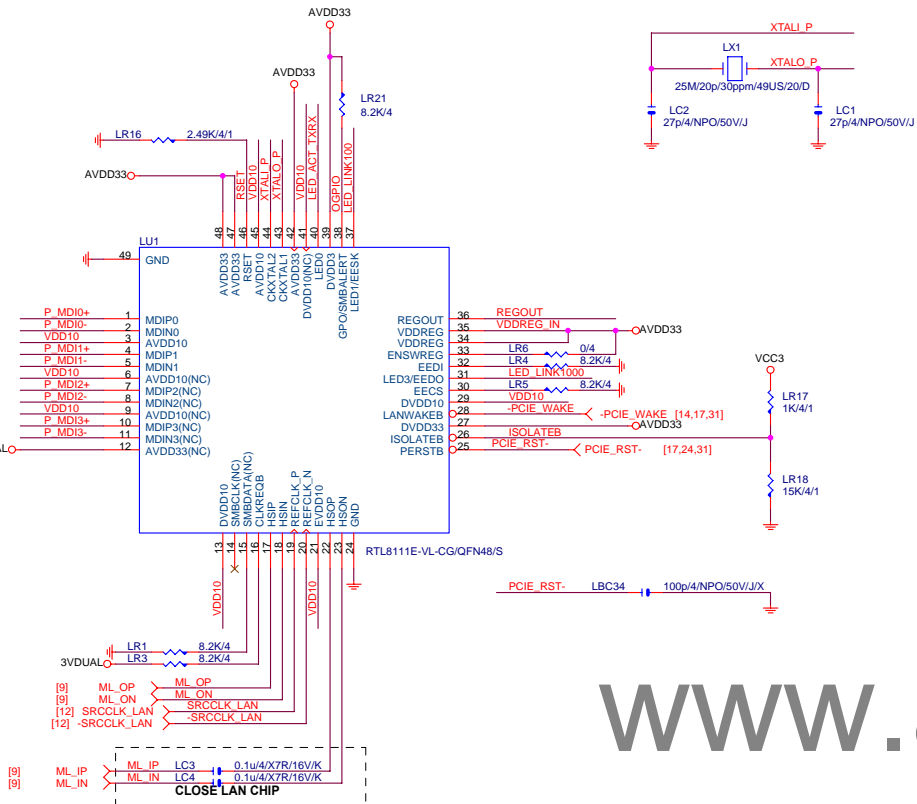




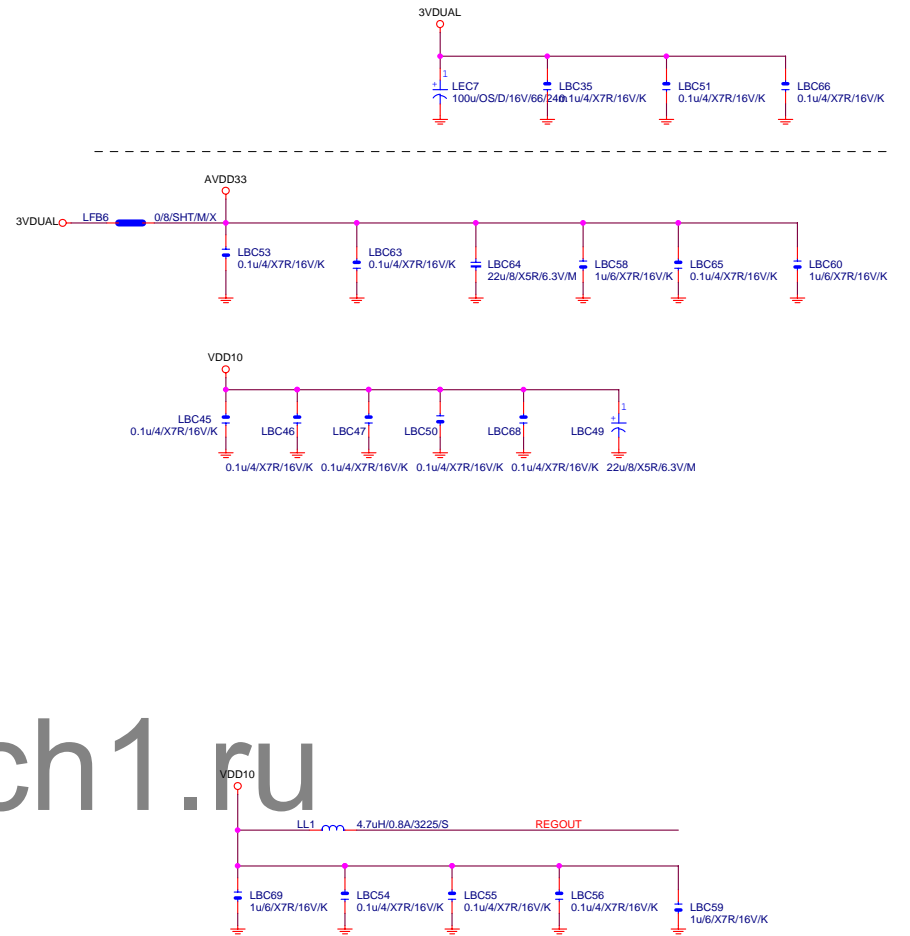
PCI SLOT 1,2



PCIE-1G LAN

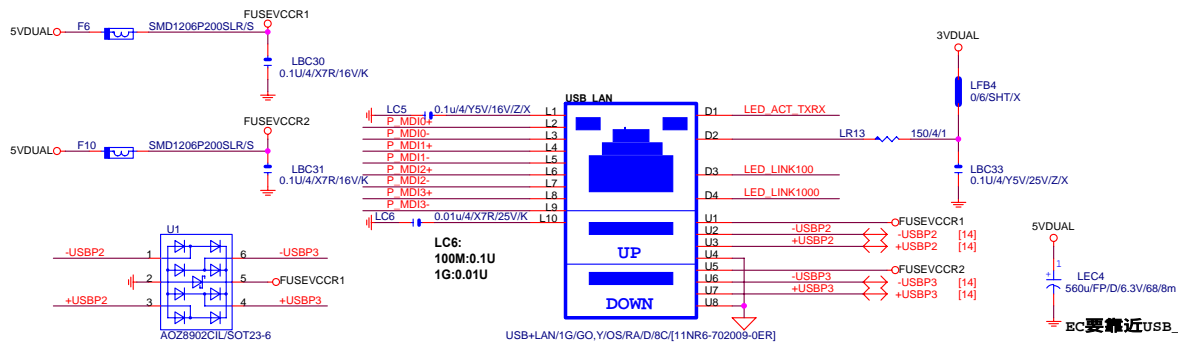


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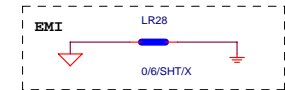


USB LAN CONNECTOR

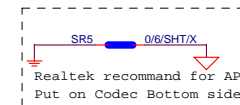
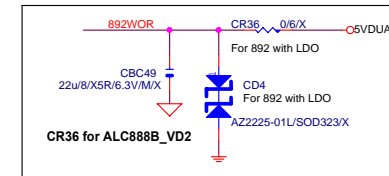
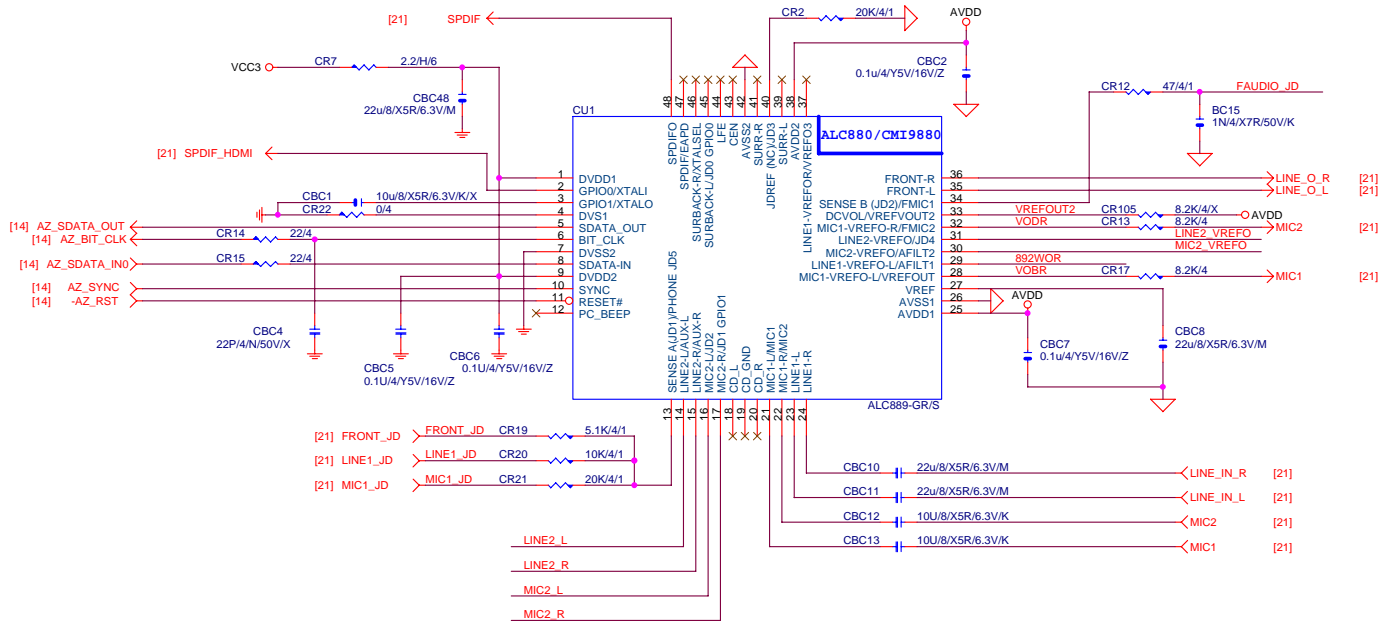
RTL8101E : L1+L10-->AVDD18+0.1u(BIOS DISABLE MDI-X FUNCTION)
1G : USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



USB_LAN



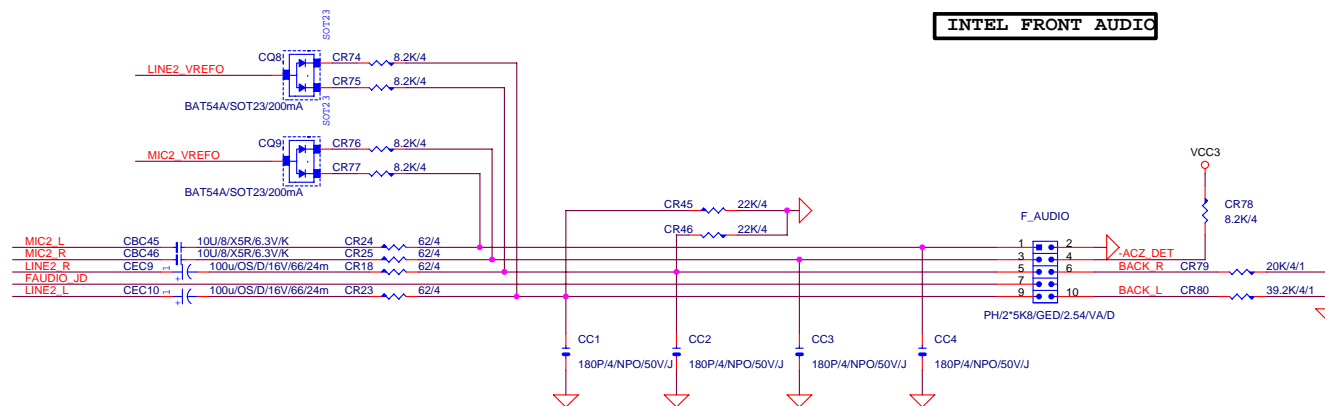
GIGABYTE			
File	REALTK RTL8111C/8101E		
Size	Document Number	Rev	
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AZALIA CODEC ALC892/ALC889/ Colay

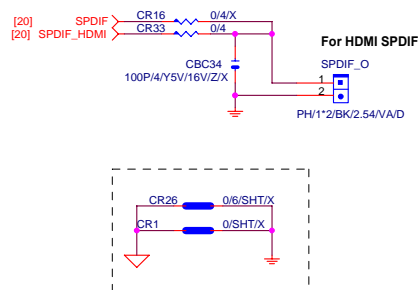
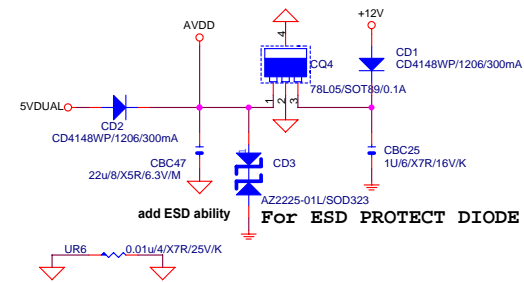
INTEL FRONT AUDIO



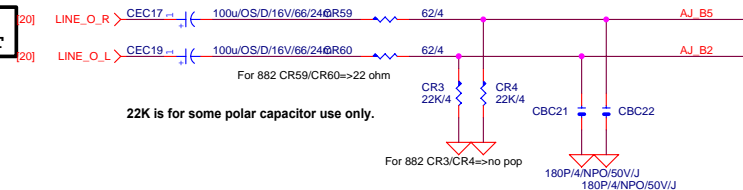
	ALC892	ALC889 Default
CR25	X	O
CBC1	10uF/X5R	X
CR2	20K/1%	20K/1%
CR10	O	O
CBC12/CBC13/CBC46/CBC45	4.7uF/X5R	10uF/X5R
CBC10/CBC11	10uF/X5R	22uF/X5R
CR24/CR25/CR18/CR23/ CR59/CR60/CR61/CR62/ CR63/CR64	75 ohm	66 ohm or lower

GIGABYTE™

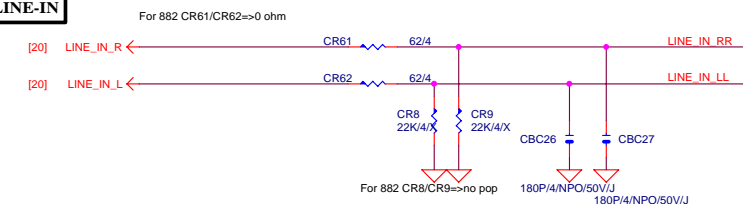
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Size	Document Number	GA-880GM-D2H	Rev
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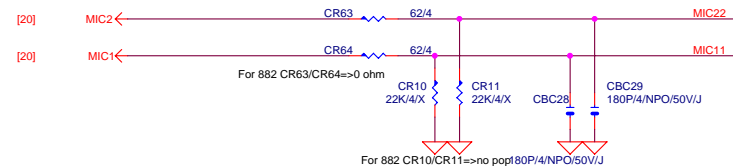
LINE OUT FRONT OUT



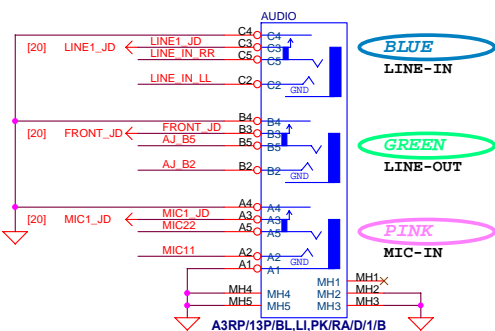
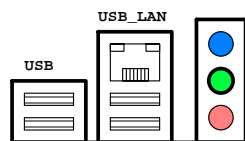
LINE-IN



MIC

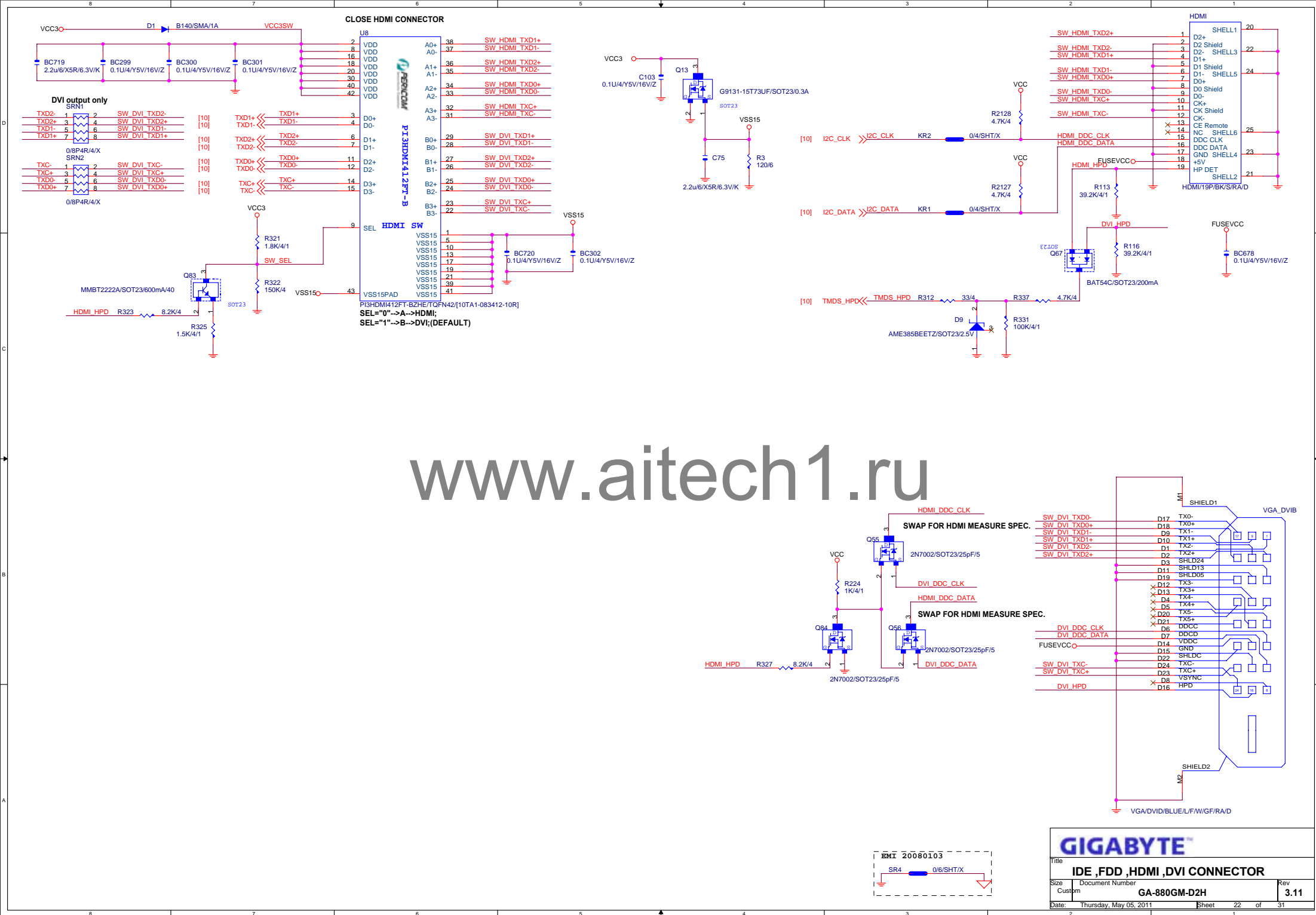


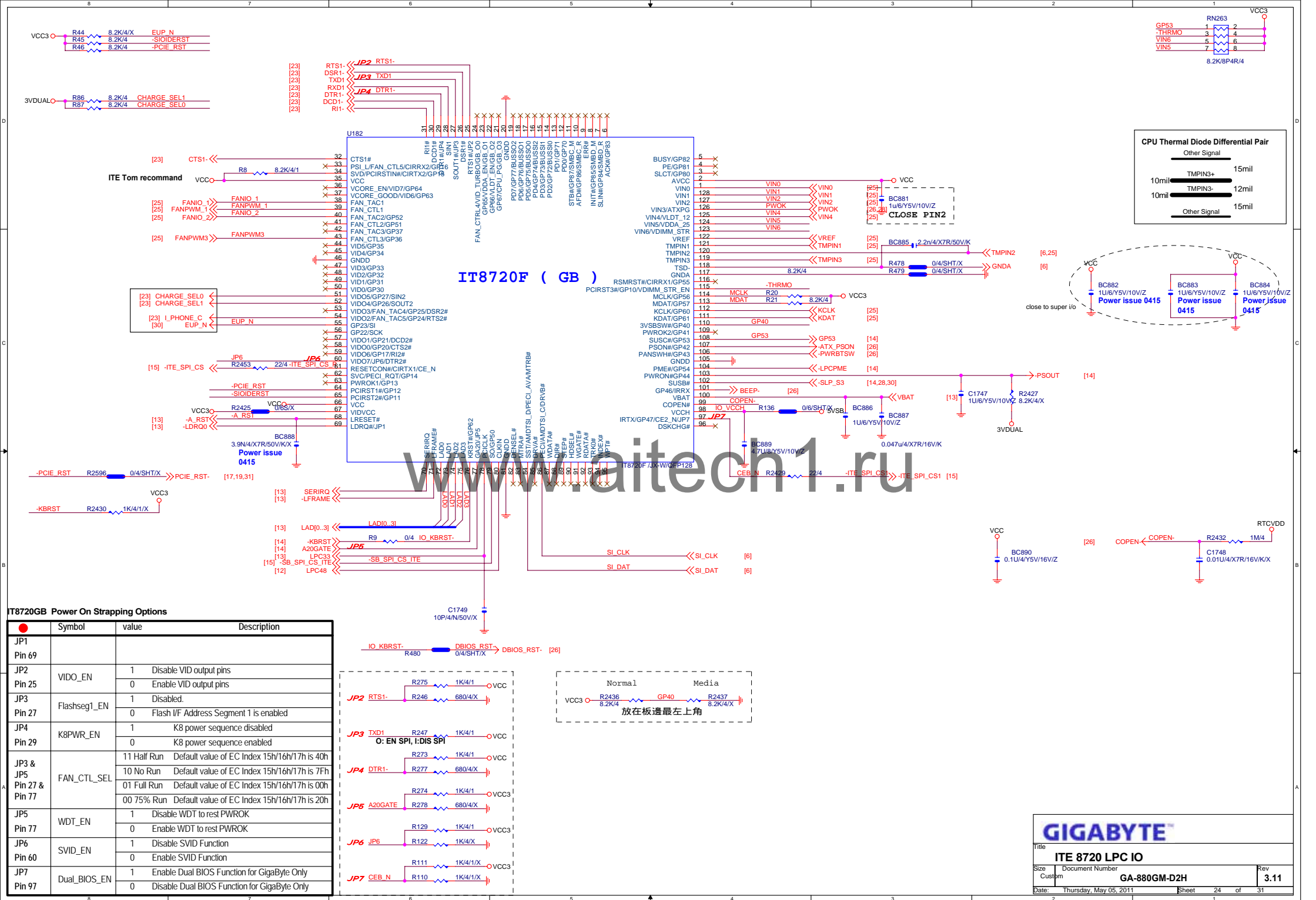
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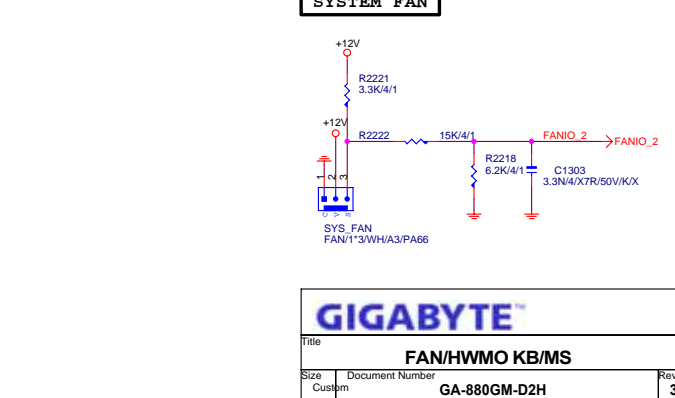
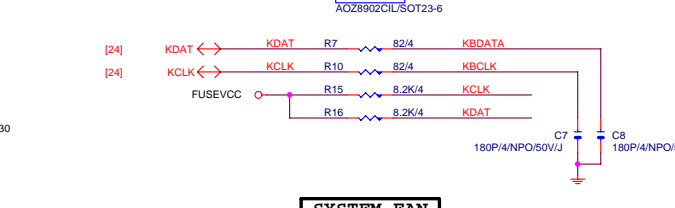
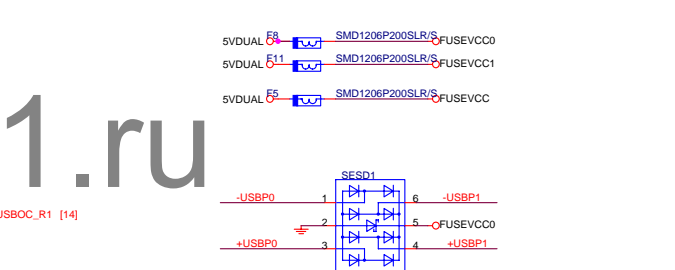
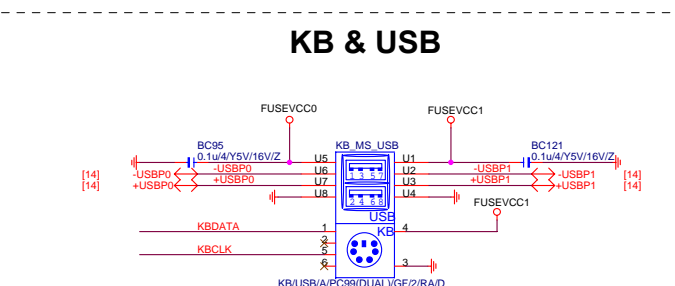
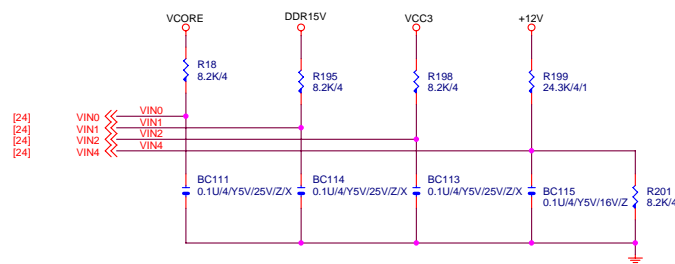
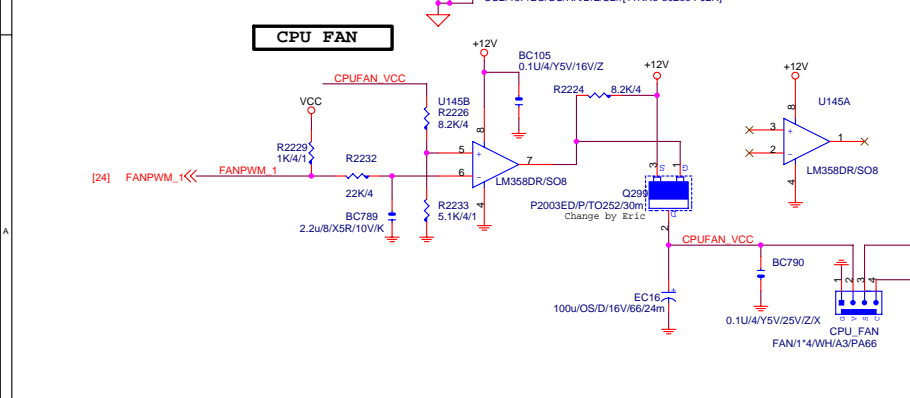
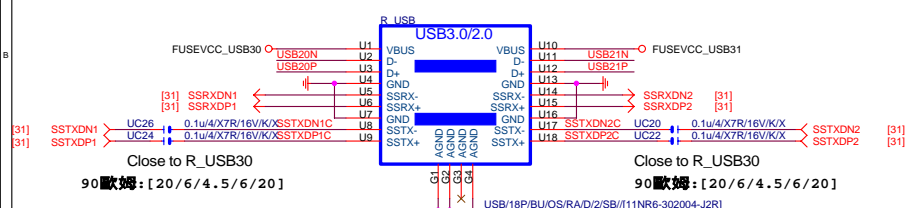
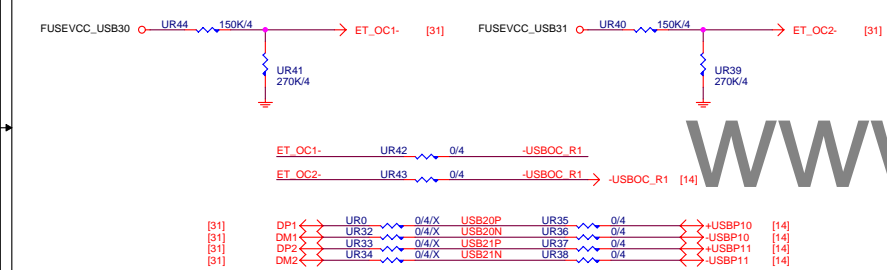
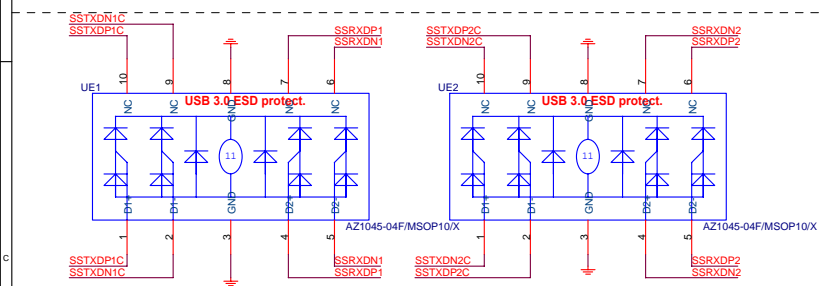
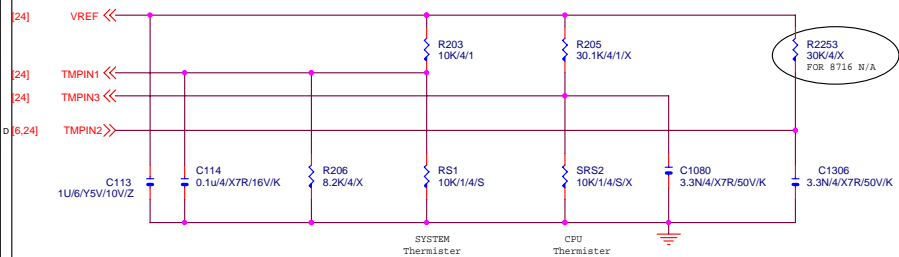
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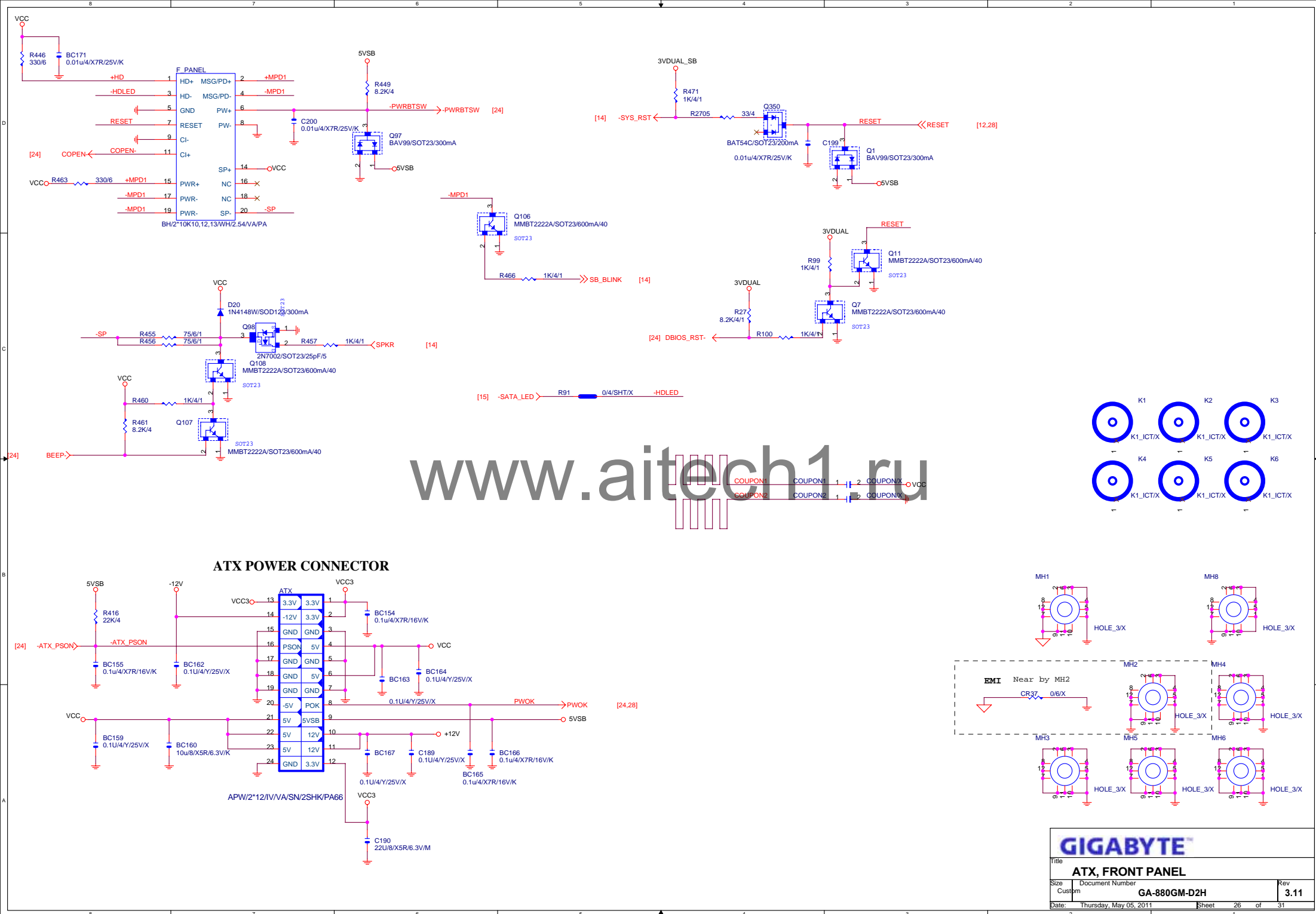
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Size	Document Number	GA-880GM-D2H	
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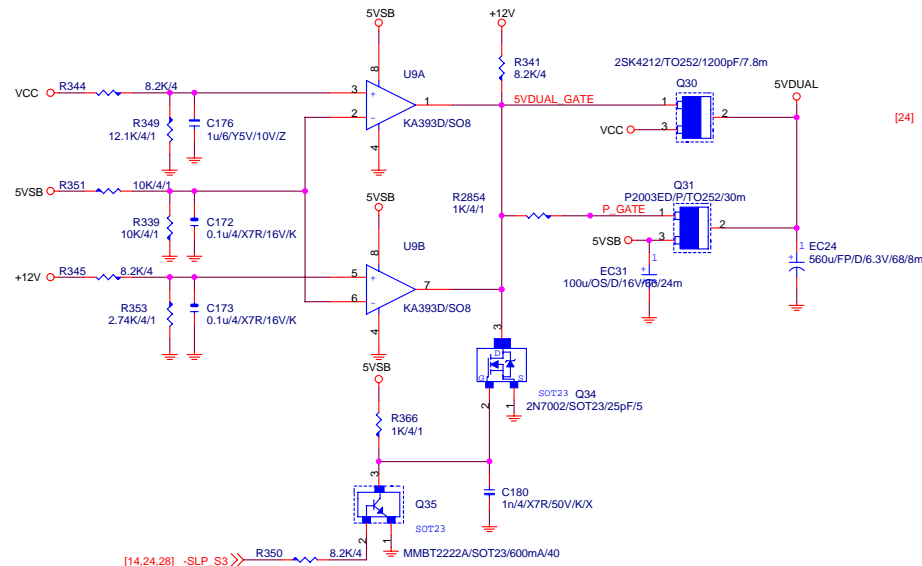
Hardware Monitor circuits







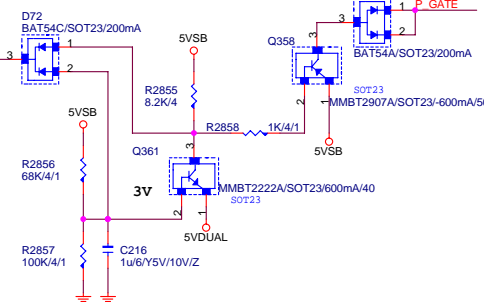
5VDUAL



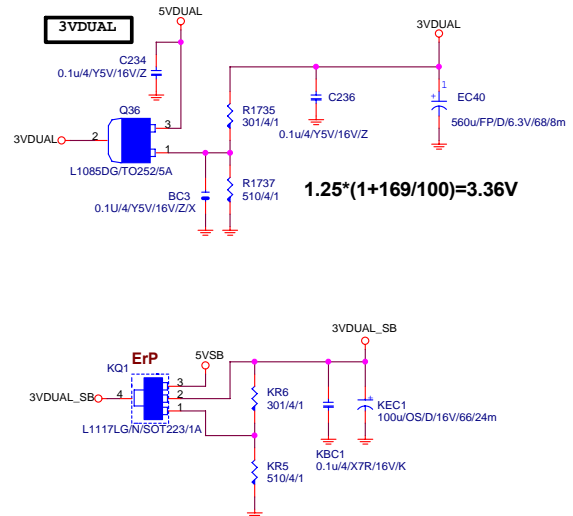
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ErP

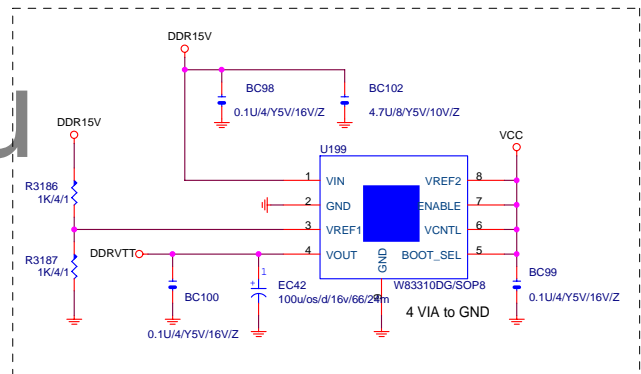
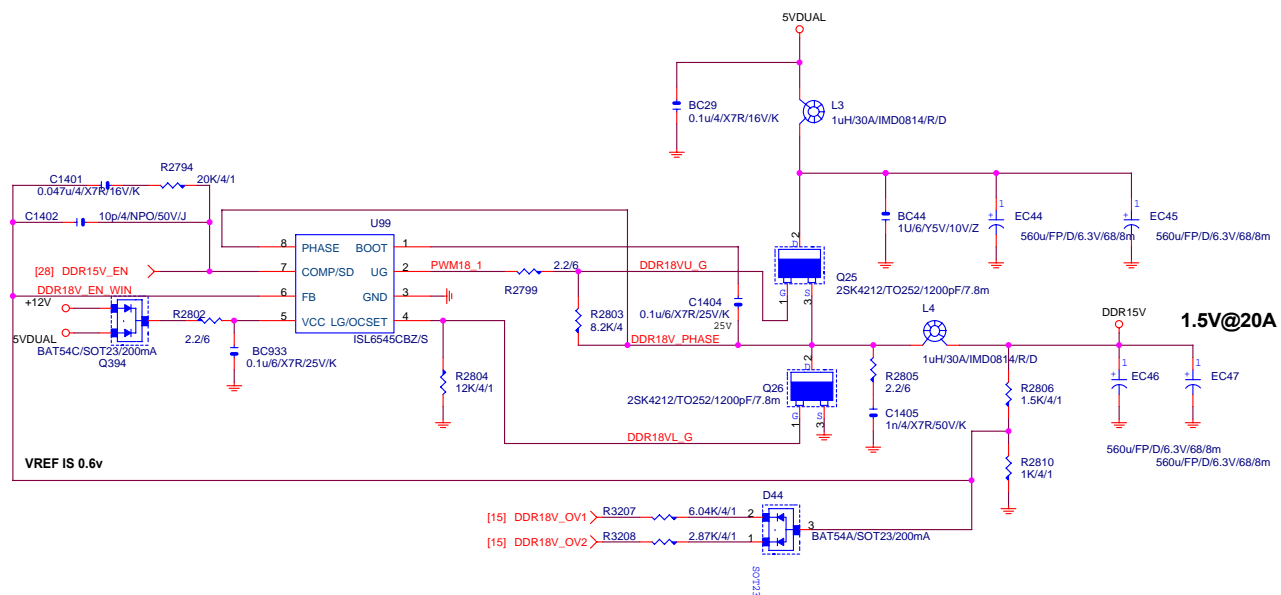
EUP_N



3VDUAL



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0.6*(1+3K/1.43K)=1.859V

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

GIGABYTE

Title: **DDRII POWER , VCC18, ErP**

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